REMARKS

Claims 1-21 are pending in the application. The Applicant's attorney has amended claims 1-10, 12-15, and 17-18, although the amendments to claims 2-3, 5-6, 8-10, 12-14, and 17 do not narrow these claims. In view of the following, all of the claims are in condition for allowance. **But if, after considering this response, the Examiner does not agree that all of the claims are allowable, then the Applicant's attorney requests that the Examiner schedule a telephone interview with the Applicant's attorney to further the prosecution of the application.**

Rejection of claims 1-21 under 35 U.S.C. § 112, Second Paragraph

The Applicant's attorney has amended the claims to address the issues with the claim language recited in the Office Action, and, therefore, requests withdrawal of this rejection.

Rejection Of Claims 1-3, 5-6, And 15 Under 35 U.S.C. § 102(b) As Being Anticipated By U.S. Patent 5,475,326 To Masuda

Claim 1

Claim 1 as amended recites a rate selector monitoring a charge on a capacitor of a filter and controlling the rate at which a phase-frequency circuit generates error-correction pulses to equal any one of more than two rates as a function of the charge on the capacitor.

For example, referring to FIGS. 5 and 9 of the patent application, a rate selector 400 monitors a charge on a filter capacitor 228 and controls the rate at which a phase-frequency circuit (combination of 200, 218, and 212) generates error-correction pulses (A, B, C, D in FIG. 9) to equal any one of more than two rates as a function of the charge on the capacitor 228. More specifically, the cycles CNT (FIG. 9) are the comparison cycles during which the PFD 200 determines the phase difference between the INPUT and OUT signals, and the

pulses A, B, C, and D are the error-correction pulses that the logic circuit 212 provides to the charge pump 220 and filter 226. When the charge on the capacitor 228 is below a predetermined threshold, the phase-frequency circuit generates the error-correction pulses at more than two rates. Specifically, the phase-frequency circuit generates the error-correction pulses at a rate equal to three CNT cycles between error-correction pulses A and B, at a rate equal to four CNT cycles between error-correction pulses B and C, at a rate equal to five CNT cycles between error-correction pulses C and D, and so on, up to a maximum rate of sixteen cycles CNT between error-corrections pulses (this represents the minimum rate of the error-correction pulses). Consequently, in this example, the error-correction pulses can have any one of sixteen rates, which are more than two rates.

In contrast, referring, *e.g.*, to FIG. 7, Masuda's circuit generates error-correction pulses to the transistors 8 and 9 at a first rate (zero frequency) when the voltage across the capacitor 13 is greater than V2 or less than V1, and generates the error-correction pulses at a second rate (frequency of signals V and R at the inputs of the phase comparator 1) when the voltage across the capacitor 13 is less than V2 and greater than V1. That is, unlike the claimed error-correction pulses, which can have any one of more than two rates, Masuda's error-correction pulses can have any one of only two rates.

Claims 2-3, 5-6, and 15

These claims are patentable by virtue of their dependencies from claim 1 as amended.

Rejection Of Claims 16-17 Under 35 U.S.C. § 103(a) As Being Unpatentable Over U.S. Patent 6,853,252 To Dickmann In View Of Masuda

These claims are patentable by virtue of their dependencies from claim 1, because neither Dickmann nor Masuda discloses or suggests a rate selector

controlling the rate at which a phase-frequency circuit generates error-correction pulses to equal any one of more than two rates as a function of the charge on a capacitor. The reasoning regarding Masuda is given above. And, referring to FIG. 3, although Dickmann discloses a delay circuit 321 that can cause a phase-frequency detector 302 to generate error-correction pulses at any one of more than two rates, Dickmann does not disclose that the rate of the error-correction pulses is a function of a charge on a capacitor.

Allowable Subject Matter

The Examiner indicated that claims 4, 7-14, and 18-19 contain patentable subject matter, and would be allowable if amended in independent form and to overcome the above-addressed rejection under 35 U.S.C. § 112. Furthermore, because the Examiner did not reject claims 20-21 in view of the prior art, the Applicant's attorney presumes that these claims would also be allowable if amended to over come the above-addressed rejection under 35 U.S.C. § 112.

CONCLUSION

In light of the foregoing remarks, claims 11, 16, and 19-21 as previously pending and claims 1-10, 12-15, and 17-18 as amended are in condition for allowance, which is respectfully requested.

In the event additional fees are due as a result of this amendment, you are hereby authorized to charge such payment to Deposit Account No. 07-1897.

Respectfully submitted,
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